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Lab 6 Notes

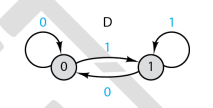
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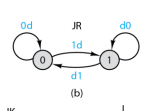
**Introduction:** Lab 6 introduces sequential circuits including D-Flip-Flops and JK-Flip-Flops. These circuits are typically used in memory devices and finite state machines. The SN747 and SN7476 and IDL-800 are used to understand how these flip flop implementations are utilized. Along with the wiring of the JK and D flip-flops the instruction register and flag register are implemented in Quartus using the D-Flip-Flop from the Altera library files. Both register will be used to realize the TRISC final project.

**Theory:**  Using the IDL-800 and chips SN7474 and SN7476 the truth table of each sequential circuit was tested and verified using the state diagrams (Figure 1 and 2)

**Figure 1:** D*-Flip-Flop state diagram*

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**Figure 2:** *JK Flip Flop State diagram*

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These chips are wired and verified with the IDL-800 using the provided table in the lab manual.

**Figure 3:** *Table of functionality of a D-Flip-Flop*

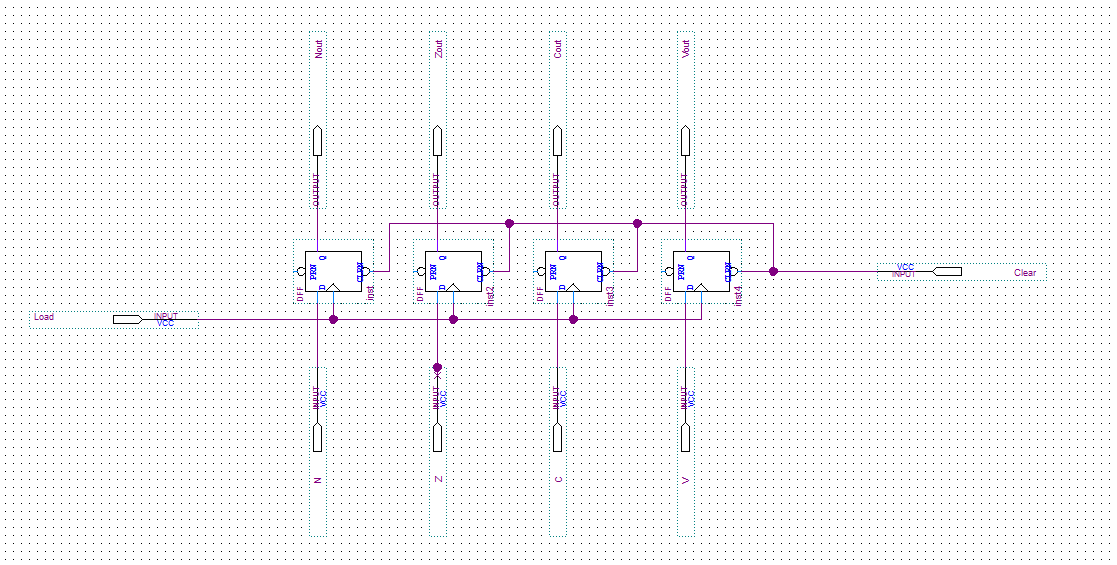
|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | Next State (Q\*) | | | | | | | |
| PreClr=00 | | PreClr=01 | | PreClr=10 | | PreClr=11 | |
| D=0 | D=1 | D=0 | D=1 | D=0 | D=1 | D=0 | D=1 |
| 0 | NA | NA | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | NA | NA | 1 | 1 | 0 | 0 | 0 | 1 |

**Figure 4:** *Table of functionality of a JK-Flip-Flop*

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | Next State | | | | | | | | | | | | | | | |
| PreClr=00 | | | | PreClr=01 | | | | PreClr=10 | | | | PreClr=11 | | | |
| JK=00 | JK=01 | JK=10 | JK=11 | JK=00 | JK=01 | JK=10 | JK=11 | JK=00 | JK=01 | JK=10 | JK=11 | JK=00 | JK=01 | JK=10 | JK=11 |
| 0 | NA | NA | NA | NA | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | NA | NA | NA | NA | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

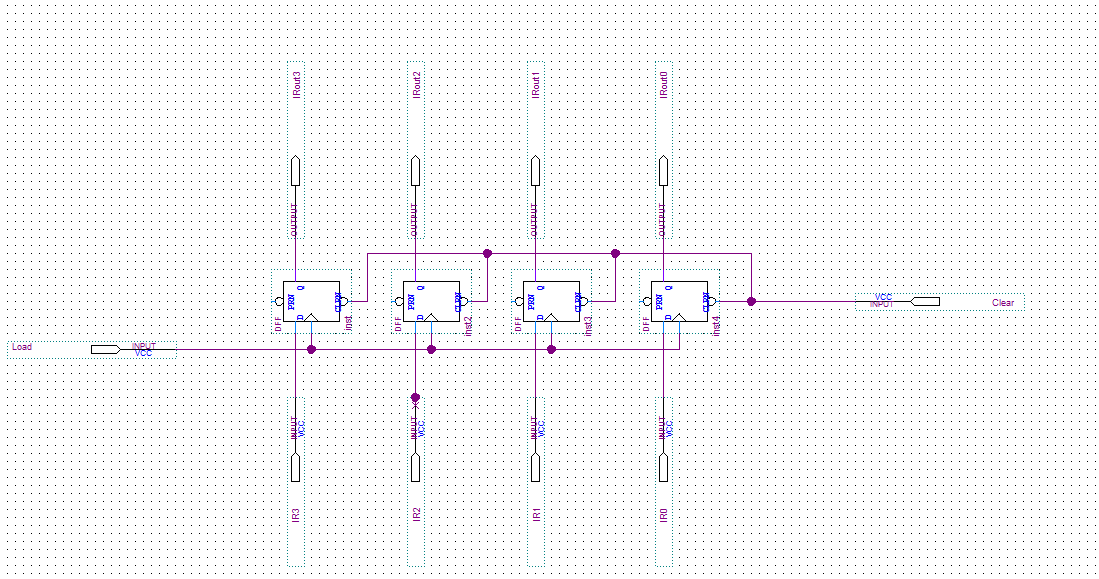
After these chips have been wired and verified the four-bit twisted ring counter is implemented on the IDL-800. When testing this unit the 4 LED’s representing the count appears to scroll from right to left. As the frequency is increased this scroll speed is increased. This function has been also verified by the lab instructor. The flag register (figure 5) and instruction register (figure 6) are then implemented in the DE1.

**Figure 5:** *Flag register implemented in Quartus*



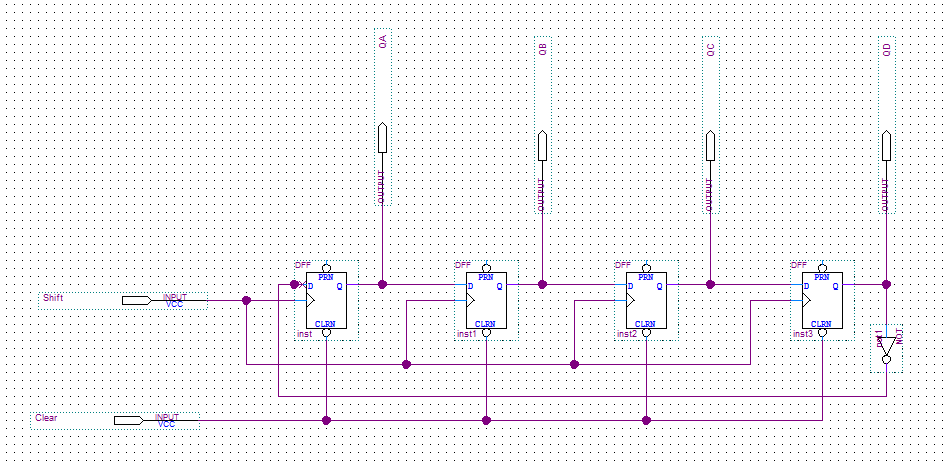
The flag register and instruction register are very similar in implementation however the pins on each register are changed to make top level assembly easier.

**Figure 6:** *Instruction Register implemented in Quartus*



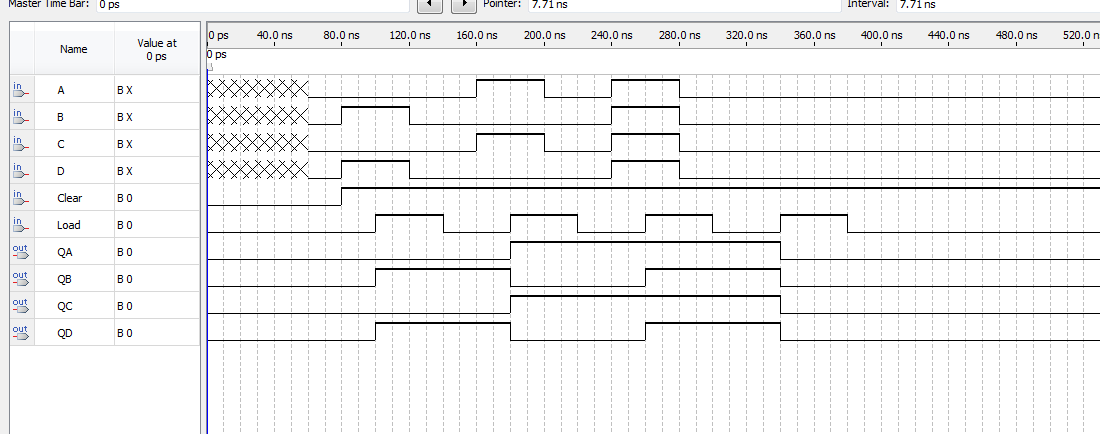
After this registers were implemented the four bit twisted ring counter was implemented into Quartus.

**Figure 7:** *Four Bit Twisted Ring Counter*

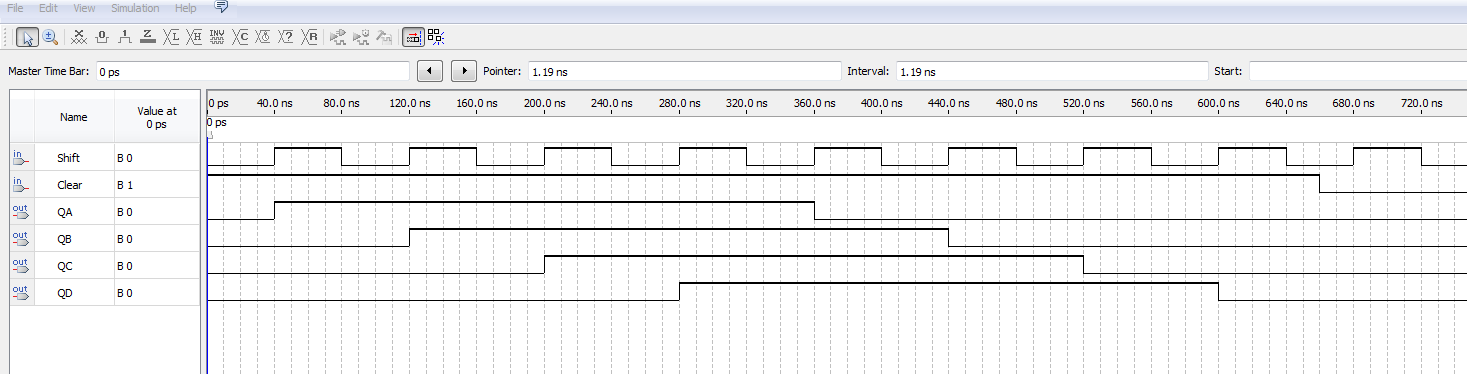
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All these modules were then tested using the waveform generator in quartus.

**Figure 8:** *Waveform for Flag and Instruction Register*



**Figure 9:** *Waveform of Twisted Ring Counter*



**Part 3:** *Answers to Part 3*

*D.* ***How does the state sequence change when clock frequency is increased?*** *The sequence change becomes increasingly faster.*

*E.* ***How many states would be in a 6-bit twisted-ring counter? N-Bit?*** *An N bit twisted counter required creates a 2n states. 6 bits requires 12 states*

**Conclusion:** Overall this lab ran smoothly a hybrid between a wiring lab and a programming lab implemented on the DE1 and the wiring on the IDL-800. All units were verified by the lab instructor.